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Design and Analasis of Hybrid C-Mos 4-Bit Parallel Adder

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Abstract: *This paper presents a low voltage and high performance 4-bit parallel adder which is used to reduce the power delay product (PDP).This technique is mainly implemented by using 1-bit hybrid full adder where we can reduce the power consumption and delay when compared with the other techniques. By considering this 1-bit hybrid full adder basic circuit we had implemented the 4-bit parallel adder. The above circuits are simulated by using tanner tool V16.0. There was improvement in speed and power delay product metric when compared with C-CMOS full adder.*

Keywords*: High Speed, Low voltage, logic structure, hybrid adder.*

I. Introduction

Adder places an important role for designing (or) implementation of any devices like laptops, pads, palmtops etc in order to implement these devices requires smaller area on silicon chip, high thought put and mainly we have to reduce the power consumption and delay. We can reduce the power consumption by scaling the supply voltage and operating frequency. But it increases the propagation delay of the system and degrades the driving capability of the design. So to design a full adder with improved power delay characteristics is of great interest. Several logic styles have been used in the past to implement the 4-bit full adder cell. Each logic style has its own advantages and disadvantages.

Standard static CMOS full adder (C-MOS) is based on the regular CMOS structure with pull up and pull down transistors. This adder provides full output voltage swing against voltage and transistor sizing. The limitations of this design are its larger area than slower speed due to the availability of PMOS devices and larger input capacitance of the static CMOS logic gates.

In order to overcome these effects we preferred the Hybrid COMS full adders. These adders are designed with a combination of more than one logic style to enhance the overall performance of the system. The main focus of hybrid logic style is to reduce the number of transistors and power dissipating nodes of the adder cell. Hybrid pass logic with static CMOS (HPSC) is an example of hybrid adder.

HPSC provides full output voltage swing and has good output drive capability. The limitation of this adder is its higher propagation delay. On the other hand, hybrid adder is a good choice in terms of power consumption and speed than HPSC but at the cost of increased number of in the design.

The main objective of this paper is to improve the different performance parameters like power, delay and transistor count of the full adder comparing with the already existing ones Based on the above mentioned parameters we had designed the proposed technique.

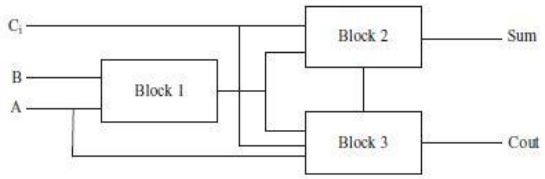


Fig. 1. Full adder module based on three logic blocks.

The above mentioned circuit is basic full adder which consists of 3 basic blocks. Block 1 has XOR/XNOR gate to generate $(A \oplus B)$ and $(A \oplus B)'$ signals and block 2 and block 3 are used as XOR blocks or multiplexers to obtain the sum and carry outputs. But the major problem of the above circuit is presence of intermediate signals. These intermediate signals are used to drive the output blocks or multiplexers and therefore responsible for higher propagation delay and power consumption. To reduce the overall propagation delay and power consumption a new full adder cell is designed with internal logic structure. The proposed structure uses inputs signal C and its complement C' to drive the output multiplexers in place of the intermediate signal. $(A \oplus B)$ and it complement $(A \oplus B)'$ The logic structure designed with input signal C also helps in reducing the overall hardware cost of the design. This logic structure consists of XOR/XNOR gates, modified NOR and NAND gates with multiplexers inserted at the output. Multiplexers are used to select the sum and carry outputs.

The resultant full adder exhibits improved PDP compared to earlier reported adder designs. Proposed design also has full output swing and is found suitable when operated at lower voltages.

The rest of the paper is organized as follows.Section 2 Implementation of 1-bit full adder Section (3) Implementation of the 4-bit hybrid cmos parallel adder. The simulation results and comparison of the entire referred and proposed full adder cells are presented in section 4.The conclusion consists of Section 5 .The references comes under Section 6.

II. Implementation of 1-Bit Full adder.

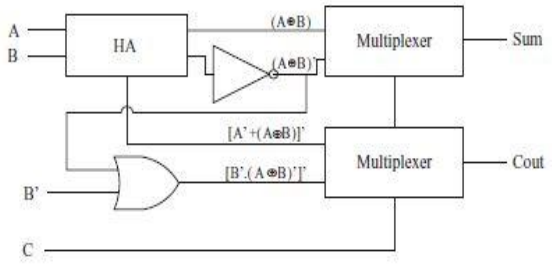


Fig. 2. Proposed internal logic structure for designing the 1-bit full adder cell.

The above block diagram represents the

Proposed 1-bit full adder. For standard CMOS the intermediate signals are driving the multiplexers so the power consumption and time delay is increasing to avoid this problem we are generating the external C input to drive the multiplexers in the proposed technique. The internal structure of the proposed technique is discussed below. In Fig. 3(a.1–a.3) three basic CMOS inverter are shown which gives the complement output of the input signals A, B and C in the form of A' B' and C' respectively. Similarly Fig. 3(b) represents the SRCPL based XOR gate and its complement in the form of XNOR gate. A and B are the input signals applied on these gates. In Fig. 3(c) and (d) modified NOR and modified NAND gates are Shown. Multiplexers required for generating the sum and carry outputs are shown in Fig. 3(e.1) and (e.2). Transmission gates are used for designing the multiplexers.

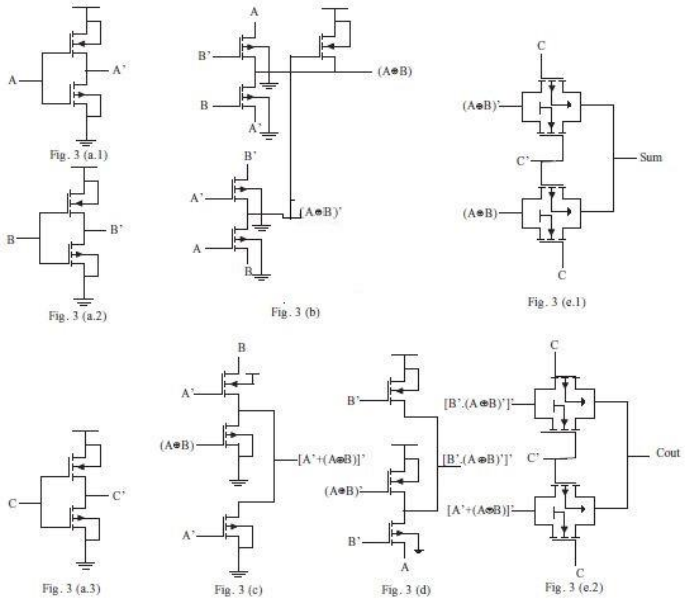


Fig. 3. Full adder designed with proposed logic structure.

Shown. Multiplexers required for generating the sum and carry outputs are shown in Fig. 3(e.1) and (e.2). Transmission gates are used for designing the multiplexers. The proposed full adder cell is realized using the logic structure of Fig. 3.

The modified NOR and modified NAND gates "as essential entities" are also proposed and shown in Fig. 3(c) and (d). A' and $(A \oplus B)$ are the inputs applied on NOR gate and outputs are shown in the form of $[A'+(A \oplus B)]'$. Similarly B' and $(A \oplus B)'$ are the inputs applied on NAND gate and output are shown in the form of $[B'.(A \oplus B)']'$.Due to this input combinations proposed NOR and proposed NAND gates require only three transistors. This makes the proposed design faster, compact and power saving. The operation of the modified NOR and NAND gates are described in Tables 2 and 3 respectively. The output combinations of these gates are selected by the output multiplexers to generate the final carry output.

Table 1
Truth table of 1-bit full adder.

A	B	C	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2
Truth table of modified NOR gate.

A'	$(A \oplus B)$	$[A'+(A \oplus B)]'$
0	0	1
0	1	0
1	0	0
1	1	0

Table 3
Truth table of modified NAND gate.

B'	$(A \oplus B)'$	$[B'.(A \oplus B)']'$
0	0	1
0	1	1
1	0	1
1	1	0

By consider above internal structure and the truth tables the implementation of the 4-bit hybrid full adder is discussed in section (3).

III. Implementation Of 4-Bit Hybrid CMOS Parallel Adder

The 4-bit full adder is implemented by using the 1-bit proposed full adder. The internal circuit of the 4-bit full adder is same as the 1-bit full adder. The schematic is shown below.
By consider this circuit as basic we implemented the 4-bit full adder by generating symbol to the circuit shown below.

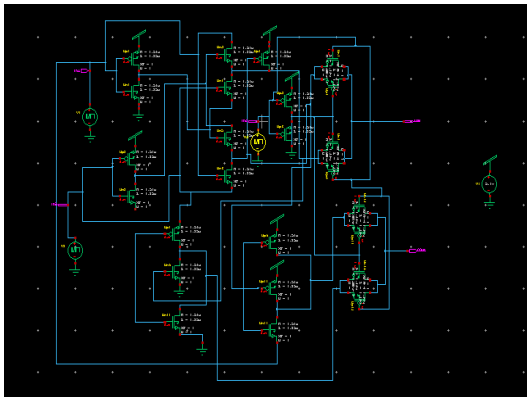


Fig 4 Proposed 1-bit full adder schematic

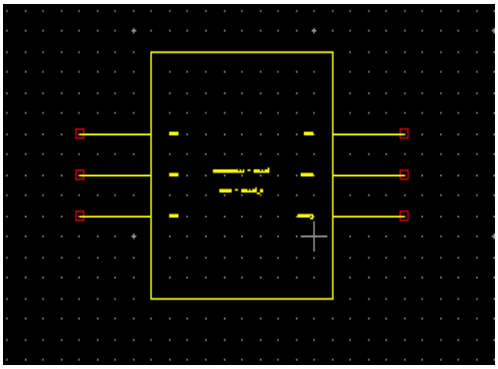


Fig 5(a) Generated Cell For 1-bit adder

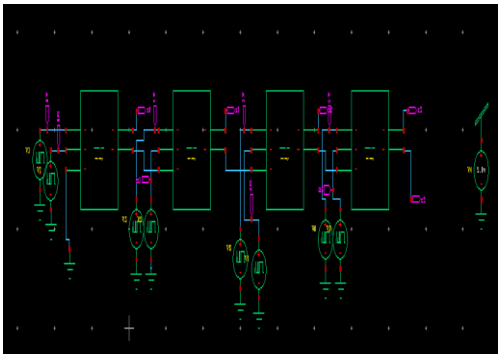


Fig 5(b) Implemented 4-bit parallel adder

The above circuit show the 4-bit hybrid parallel adder. As we know that full adder consists of three inputs A, B, C and the outputs are Sum and Carry.
Here the inputs A and B are the inputs generated by the bit sources and C is kept to ground and the output obtained from the first symbol output sum and carry. Here the input C is given to the ground because the output Carry which is generated from the first circuit is given as input to the second symbol.
Hence the C input is internally generated. The same process is repeated for the next two symbols and final out COUT will be obtain.

Average powerand time	0.4v	0.6v	1.0v	1.2v
4-bit power	4.357713e-007 W	4.579816e-006 W	9.152671e-005 W	1.904820e-004 W
4-bit time delay	10.8470n	708.3492p	764.3054p	764.4388p

Table 3 power and time delay of 4-bit full adder

Finally this circuit is implemented by the using the hybrid adders in order to reduce the power consumption and delay. As we mentioned above that the comparison of different circuits are done on the basis of power consumption and delay are mentioned in the following section (4)

IV. Simulation and Comparison Results

The simulation of the circuits C-CMOS, HPSC, Hybrid CMOS and proposed full adder are carried out with TANNER TOOL with 250nm technology. The comparison is done by various voltages ranging from 0.4v to 1.2v with a frequency 100 MHz

The size of each full adder is taken as the same as those reported in literature. The proposed full adder designed with internal structure is compared in terms of power consumption, propagation delay with existed

Full adders the comparison is listed in the below table.

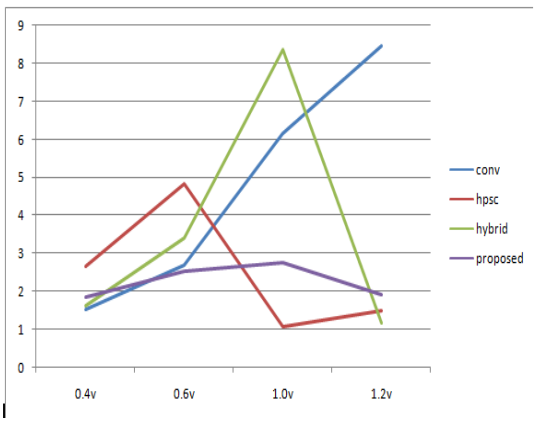
Average power	0.4v	0.6v	1.0v	1.2v
conventional	1.523651e-011 W	2.689752e-011 W	6.181055e-011 W	8.473146e-011 W
Hpsc	2.689752e-011 W	4.832020e-011 W	1.096175e-010 W	1.509008e-010 W
Hybrid	1.638373e-011 W	3.390952e-011 W	8.369939e-011 W	1.177461e-010 W
Proposed	1.856110e-004 W	2.545996e-004 W	2.777536e-004 W	1.906943e-004 W

Table 4 power comparison

Time Delay	0.4V	0.6V	1.0V	1.2V
conventional	-050.2449n	-68.8584n	-70.5867n	-70.6671n
Hpsc	9.3801n	-59.3206n	-59.8630n	-70.5804n
Hybrid	9.6409n	142.3547p	-174.0635p	-238.5572p
Proposed	-10.8488n	-700.8236p	-700.5852p	-701.2160p

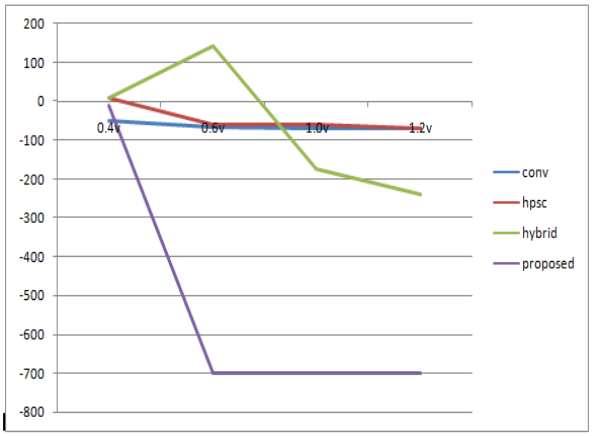
Table 5 Compared Time Delay

Observing the conventional and proposed there was a drastic change is observed the proposed full adder achieve 69.36% reduction in propagation delay as well as in the power. By comparing the HPSC as well as the Hybrid Full adder with proposed technique 60% to 70% of reduction of delay and power consumption took place. Hence based on these results we had implemented the 4-bit parallel adder and the obtained power and time results are mentioned above. For the different voltages the different time delays occur. The graphs are shown below. The proposed adder operates successfully on low voltages and provides full output voltage swing and thus exhibits smaller power delay at low voltages. This makes the proposed design a good candidate for low voltage and high speed VLSI applications. For the obtained voltages the comparison graph is shown below.



Graph (1) power Consumption

By observing the above two graphs for power consumption as well as time delay there was drastical variation by comparing with other techniques.



Graph (2) Time Delay

V. Conclusion

In this paper, 4-bit high performance full adder cells based on efficient internal logic structure have been presented. Spectre simulations are carried out on TANNER 250-nm technologies to evaluate the new design and existing designs. Results show that the proposed design has high performance and best Power Delay in comparison with many existing full adder cells. Consequently, this new design is found appropriate at low voltages and has good output levels. This shows that proposed design can be a good choice in the future at scaled technology or nano scaling. It is also verified through simulation results that the proposed design perform well under the projected variations in supply voltage and temperature.

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